conductive layer **81** may be formed by sputtering or thermal evaporating process, wherein the thickness of the transparent conductive layer **81** may be 300~1000 Å, and the material of the transparent conductive layer **81** may be tin-doped indium oxide film (ITO), or other oxide or metal. The transparent conductive layer **81** is used for forming a pixel electrode which is connected with the drain electrode via the via-hole **72**.

It should be noted that, the same parts in FIG. **6** to FIG. **8** are presented by the same reference numbers.

Another embodiment of the present invention provides an array substrate which is manufactured by the above method for manufacturing an array substrate.

Since the array substrate according to the embodiment of the present invention is manufactured by the above method for manufacturing an array substrate, and in the above method for manufacturing an array substrate, an adhesion enhancement layer, a copper-bearing metal layer and a photoresist layer are sequentially formed on a substrate, then a reserved region and a removal region are respectively formed by performing exposure and development on the photoresist layer using a mask plate, wherein the reserved region corresponds to the pattern forming region, then the adhesion enhancement layer, the copper-baring metal layer and the photoresist layer in the removal region are simultaneously processed by a single wet etching process, then a dry etching process is followed and the photoresist layer is stripped off, to form a patterned adhesion enhancement layer and a patterned copper-bearing metal layer wherein the adhesion enhancement layer can enhance adhesion of the copper-bearing metal layer to the substrate, and at least one of the gate electrode, the gate line, the source electrode, the drain electrode, and the data line can be formed by the copper-bearing metal layer, since the resistance of copper is relatively low thereby the Issue due to the signal delay of the gate line and the data line in a large-size display device can be avoided, and the quality of the image displayed on the display device can be improved. Moreover, in the patterning process for forming the patterned copper-bearing metal layer and the patterned adhesion enhancement layer, the etching procedure in which a wet etching process is first performed and a dry etching process is then performed, is employed, thereby the problem that there is residual adhesion enhancement layer after the wet etching process can be effectively solved, thus a good cross-section of the patterned copper-bearing metal layer is formed, and the issue relating to thin film covering due to the poor cross-section of the patterned copper-bearing metal layer is solved.

Another embodiment of the present invention provides a display device comprising the array substrate according to the above embodiment of the present invention. The display device may be a liquid crystal panel, an electronic paper, an OLED panel, a liquid crystal television, a liquid crystal display, a digital photo frame, a mobile telephone, a tablet personal computer, or any product or component with a display function.

Since the above array substrate is employed in the display device according to the embodiment of the present invention, the issue of signal delay of the gate lines and the data lines in a largo-size display device can be avoided, and the pixels can be fully charged, thereby an uniform brightness is obtained, and the contrast of the display device and the quality of the image displayed on the display device are improved.

It should be understood that, the above implementations are only used to explain the principle of the present invention, but not to limit the present invention, the person skilled in the art can make various variations and modifications without departing from the spirit and scope of the present invention, therefore, all equivalent technical solutions fall within the scope of the present invention, and the protection scope of the present invention should be defined by the claims.

The invention claimed is:

1. A method for manufacturing an array substrate, comprising a step:

(1) sequentially forming a first adhesion enhancement layer, a first copper-bearing metal layer and a photoresist layer on a substrate, and respectively forming a reserved region and a removal region by performing exposure and development on the photoresist layer using a mask plate, wherein the reserved region corresponds to a pattern forming region; simultaneously processing the first adhesion enhancement layer, the first copper-bearing metal layer and the photoresist layer in the removal region by a single wet etching process to completely remove the first adhesion enhancement layer, the first copper-bearing metal layer, and the photoresist layer in the removal region, thus forming a first adhesion enhancement intermediate layer corresponding to the first adhesion enhancement layer, a first copper-bearing metal intermediate layer corresponding to the first copper-bearing metal layer, and the photoresist layer on the first copper-bearing metal intermediate layer in the reserved region, wherein the width of the formed first adhesion enhancement intermediate layer is larger than the width of the formed first copper-bearing metal intermediate layer, so that the first adhesion enhancement intermediate layer forms a step structure with respect to the first copper-bearing metal intermediate layer; and simultaneously processing the first adhesion enhancement intermediate layer, the first copper-bearing metal intermediate layer and the photoresist layer thereon in the reserved region by a dry etching process to remove the step structure, then stripping off the photoresist layer, to form a patterned first adhesion enhancement layer and a patterned first copper-bearing metal layer respectively, wherein the first adhesion enhancement layer is a metal layer for enhancing adhesion of the first copper-bearing metal layer to the substrate.

2. The method of claim **1**, wherein the patterned first copper-bearing metal layer is a pattern comprising gate electrodes.

3. The method of claim **2**, wherein the pattern comprising gate electrodes comprises gate electrodes and gate lines formed in the same layer.

4. The method of claim **1**, wherein the patterned first copper-bearing metal layer is a pattern comprising source electrodes and drain electrodes.

5. The method of claim **4**, wherein the pattern comprising source electrodes and drain electrodes comprises source electrodes, drain electrodes and data lines formed in the same layer.

6. The method of claim **1**, wherein the material of the first copper-bearing metal layer is copper or copper alloy.

7. The method of claim **1**, wherein the material of the first adhesion enhancement layer is any one of tungsten, tantalum, titanium, molybdenum, molybdenum alloy and titanium alloy.

8. The method of claim **1**, wherein the thickness of the first adhesion enhancement layer is 100~1000 Å, and the thickness of the first copper-bearing metal layer is 1500~5000 Å.